FAIRCHILD SEMICONDUCTOR™

October 1987
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MM74C925 • MM74C926 • MM74C927 • MM74C928 4-Digit Counters with Multiplexed 7-Segment Output Drivers

General Description

The MM74C925, MM74C926, MM74C927 and MM74C928 CMOS counters consist of a 4-digit counter, an internal output latch, NPN output sourcing drivers for a 7-segment display, and an internal multiplexing circuitry with four multiplexing outputs. The multiplexing circuit has its own free-running oscillator, and requires no external clock. The counters advance on negative edge of clock. A HIGH signal on the Reset input will reset the counter to zero, and reset the carry-out LOW. A LOW signal on the Latch Enable input will latch the number in the counters into the internal output latches. A HIGH signal on Display Select input will select the number in the counter to be displayed; a LOW level signal on the Display Select will select the number in the output latch to be displayed.

The MM74C925 is a 4-decade counter and has Latch Enable, Clock and Reset inputs.

The MM74C926 is like the MM74C925 except that it has a display select and a carry-out used for cascading counters. The carry-out signal goes HIGH at 6000, goes back LOW at 0000.

The MM74C927 is like the MM74C926 except the second most significant digit divides by 6 rather than 10. Thus, if the clock input frequency is 10 Hz, the display would read tenths of seconds and minutes (i.e., 9:59.9).

The MM74C928 is like the MM74C926 except the most significant digit divides by 2 rather than 10 and the carry-out is an overflow indicator which is HIGH at 2000, and it goes back LOW only when the counter is reset. Thus, this is a 3½-digit counter.

Features

- Wide supply voltage range: 3V to 6V
- Guaranteed noise margin: 1V
- High noise immunity: 0.45 V_{CC} (typ.)
- High segment sourcing current: 40 mA @ V_{CC} − 1.6V, V_{CC} = 5V
- Internal multiplexing circuitry

Design Considerations

Segment resistors are desirable to minimize power dissipation and chip heating. The DS75492 serves as a good digit driver when it is desired to drive bright displays. When using this driver with a 5V supply at room temperature, the display can be driven without segment resistors to full illumination. The user must use caution in this mode however, to prevent overheating of the device by using too high a supply voltage or by operating at high ambient temperatures.

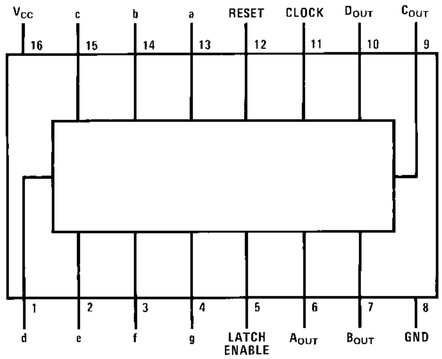
The input protection circuitry consists of a series resistor, and a diode to ground. Thus input signals exceeding V_{CC} will not be clamped. This input signal should not be allowed to exceed 15V.

Ordering Code:

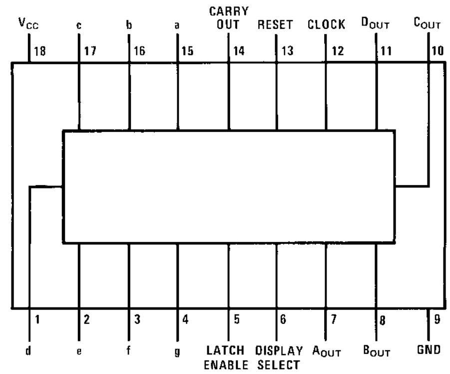
Order Number	Package Number	Package Description
MM74C925N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide
MM74C926N	N18A	18-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide
MM74C927N	N18A	18-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide
MM74C928N	N18A	18-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide

Connection Diagrams

Pin Assignments for DIP



Top View
MM74C925



Top View
MM74C926, MM74C927, MM74C928

Functional Description

Reset — Asynchronous, active high

Display Select — High, displays output of counter
Low, displays output of latch

Latch Enable — High, flow through condition
Low, latch condition

Clock —Negative edge sensitive

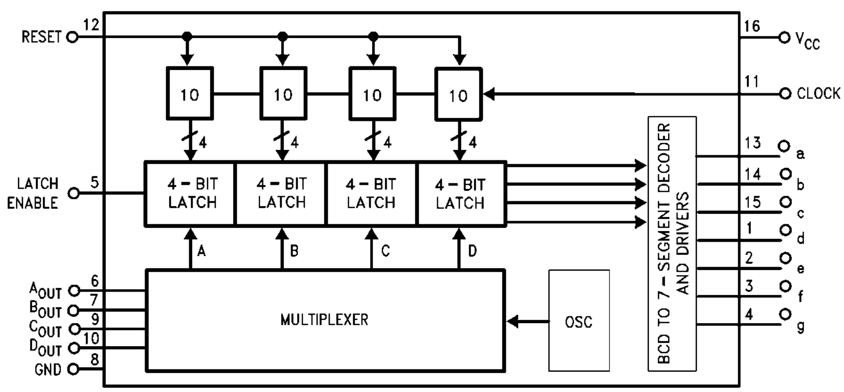
Segment Output — Current sourcing with 40 mA @V_{OUT} = V_{CC} – 1.6V (typ.) Also, sink capability = 2 LTTL loads

Digit Output — Current sourcing with 1 mA @V_{OUT} = 1.75V. Also, sink capability = 2 LTTL loads

Carry-Out — 2 LTTL loads. See carry-out waveforms.

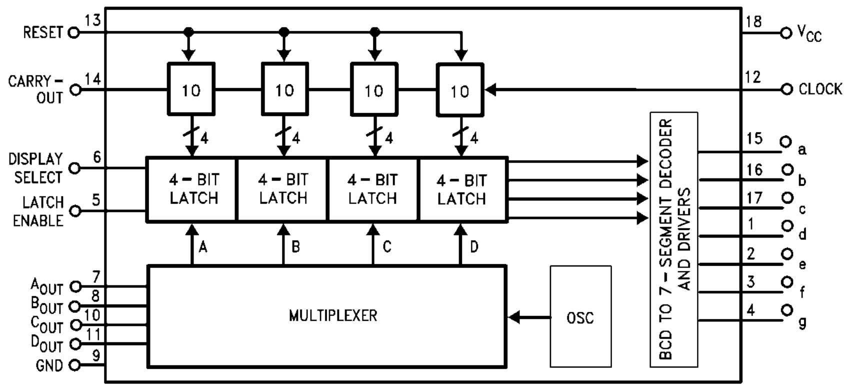
Logic Diagrams

MM74C925

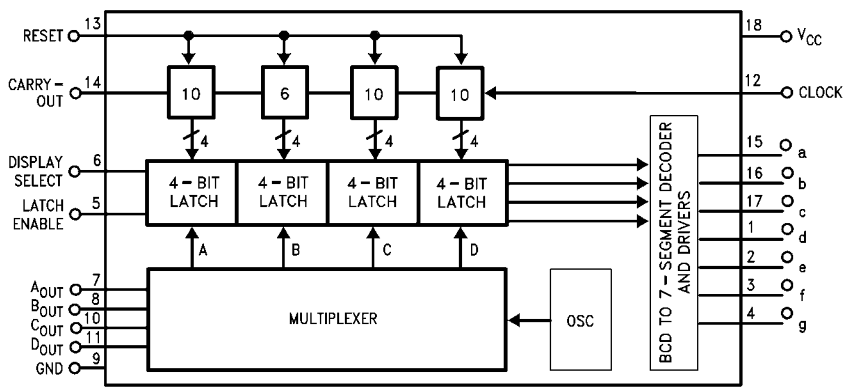


Logic Diagrams (Continued)

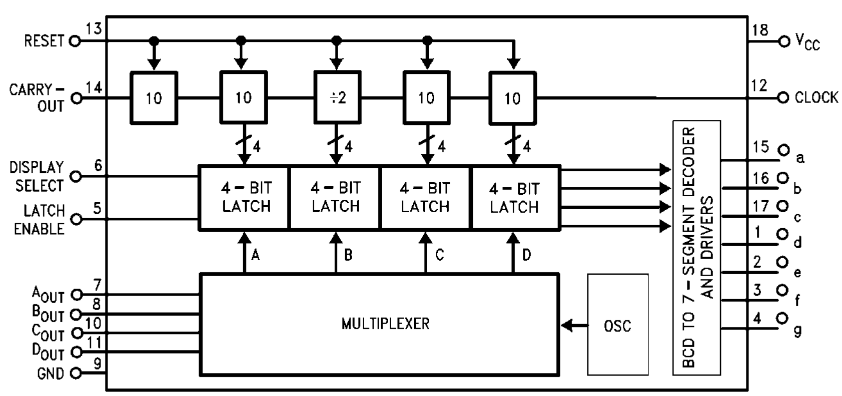
MM74C926



MM74C927



MM74C928



Absolute Maximum Ratings (Note 1)

Voltage at Any Output Pin	GND – 0.3V to V_{CC} + 0.3V
Voltage at Any Input Pin	GND – 0.3V to +15V
Operating Temperature Range (T_A)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Power Dissipation (P_D)	Refer to $P_{D(MAX)}$ vs T_A Graph
Operating V_{CC} Range	3V to 6V
V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	260°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics table provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply at –40°C ≤ t_j ≤ + 85°C, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V	3.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V			1.5	V
$V_{OUT(1)}$	Logical "1" Output Voltage (Carry-Out and Digit Output Only)	V_{CC} = 5V, I_O = –10 µA	4.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = 10 µA			0.5	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5V, V_{IN} = 15V		0.005	1	µA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5V, V_{IN} = 0V	–1	–0.005		µA
I_{CC}	Supply Current	V_{CC} = 5V, Outputs Open Circuit, V_{IN} = 0V or 5V		20	1000	µA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 4.75V	V_{CC} – 2			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage (Carry-Out and Digit Output Only)	V_{CC} = 4.75V, I_O = –360 µA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 4.75V, I_O = 360 µA			0.4	V
OUTPUT DRIVE						
V_{OUT}	Output Voltage (Segment Sourcing Output)	I_{OUT} = –65 mA, V_{CC} = 5V, T_j = 25°C	V_{CC} – 2	V_{CC} – 1.3		V
		I_{OUT} = –40 mA, V_{CC} = 5V T_j = 100°C	V_{CC} – 1.6	V_{CC} – 1.2		V
		T_j = 150°C	V_{CC} – 2	V_{CC} – 1.4		V
R_{ON}	Output Resistance (Segment Sourcing Output)	I_{OUT} = –65 mA, V_{CC} = 5V, T_j = 25°C		20	32	Ω
		I_{OUT} = –40 mA, V_{CC} = 5V T_j = 100°C		30	40	Ω
		T_j = 150°C		35	50	Ω
	Output Resistance (Segment Output) Temperature Coefficient			0.6	0.8	%/°C
I_{SOURCE}	Output Source Current (Digit Output)	V_{CC} = 4.75V, V_{OUT} = 1.75V, T_j = 150°C	–1	–2		mA
I_{SOURCE}	Output Source Current (Carry-Out)	V_{CC} = 5V, V_{OUT} = 0V, T_j = 25°C	–1.75	–3.3		mA
I_{SINK}	Output Sink Current (All Outputs)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_j = 25°C	1.75	3.6		mA
θ_{jA}	Thermal Resistance	MM74C925: (Note 2)		75	100	°C/W
		MM74C926, MM74C927, MM74C928		70	90	°C/W

Note 2: θ_{jA} measured in free-air with device soldered into printed circuit board.

AC Electrical Characteristics (Note 3)

$T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

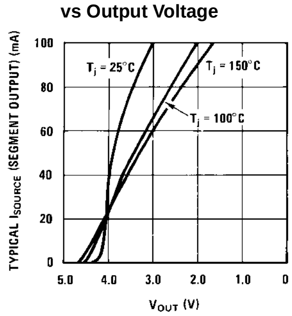
Symbol	Parameter	Conditions		Min	Typ	Max	Units
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5V$,	$T_j = 25°C$	2	4		MHz
		Square Wave Clock	$T_j = 100°C$	1.5	3		MHz
t_r, t_f	Maximum Clock Rise or Fall Time	$V_{CC} = 5V$				15	µs
t_{WR}	Reset Pulse Width	$V_{CC} = 5V$	$T_j = 25°C$	250	100		ns
			$T_j = 100°C$	320	125		ns
t_{WLE}	Latch Enable Pulse Width	$V_{CC} = 5V$	$T_j = 25°C$	250	100		ns
			$T_j = 100°C$	320	125		ns
$t_{SET(CK, LE)}$	Clock to Latch Enable Set-Up Time	$V_{CC} = 5V$	$T_j = 25°C$	2500	1250		ns
			$T_j = 100°C$	3200	1600		ns
t_{LR}	Latch Enable to Reset Wait Time	$V_{CC} = 5V$	$T_j = 25°C$	0	–100		ns
			$T_j = 100°C$	0	–100		ns
$t_{SET(R, LE)}$	Reset to Latch Enable Set-Up Time	$V_{CC} = 5V$	$T_j = 25°C$	320	160		ns
			$T_j = 100°C$	400	200		ns
f_{MUX}	Multiplexing Output Frequency	$V_{CC} = 5V$		1000			Hz
C_{IN}	Input Capacitance	Any Input (Note 4)		5			pF

Note 3: AC Parameters are guaranteed by DC correlated testing.

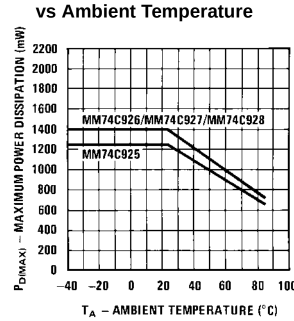
Note 4: Capacitance is guaranteed by periodic testing.

Typical Performance Characteristics

Typical Segment Current vs Output Voltage

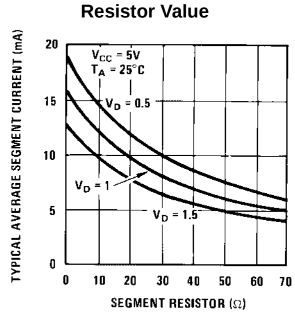


Maximum Power Dissipation vs Ambient Temperature



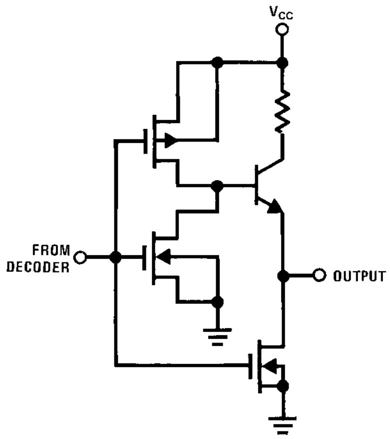
Note: V_D = Voltage across digit driver

Typical Average Segment Current vs Segment Resistor Value

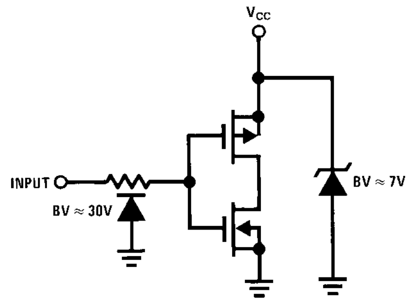


Typical Performance Characteristics (Continued)

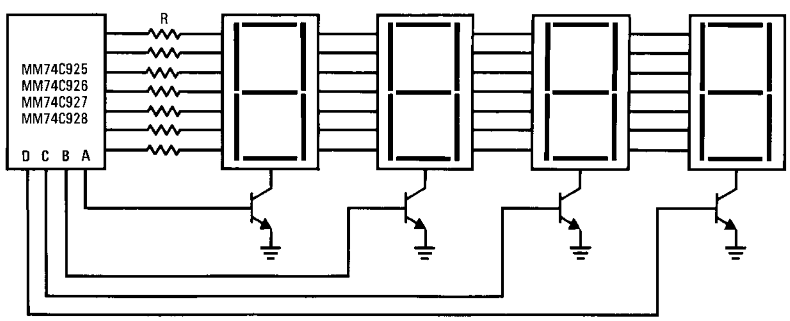
Segment Output Driver



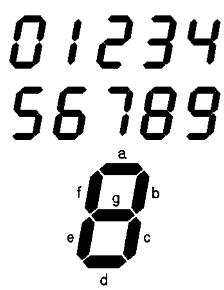
Input Protection



Common Cathode LED Display

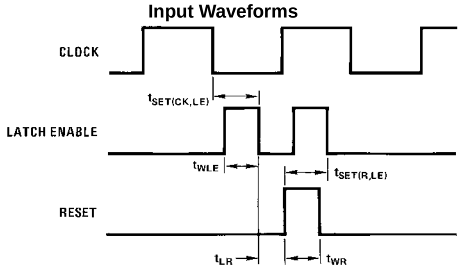


Segment Identification

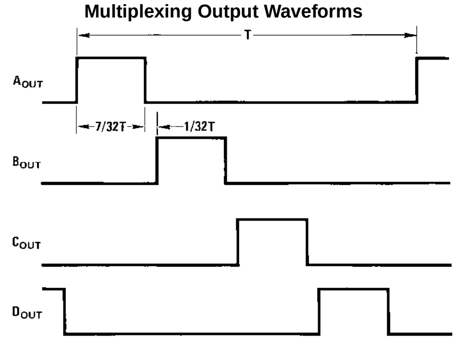


Switching Time Waveforms

Input Waveforms

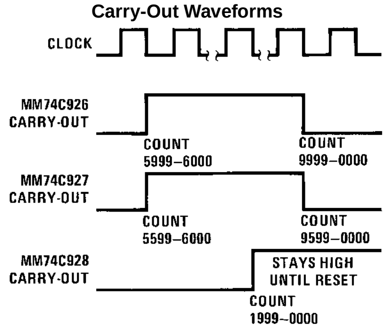


Multiplexing Output Waveforms

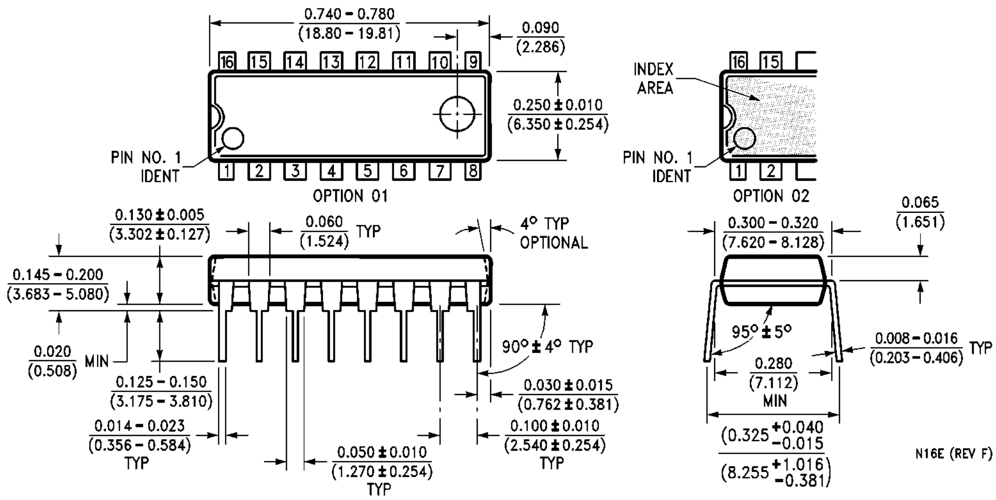


$T = 1/f_{MUX}$

Carry-Out Waveforms

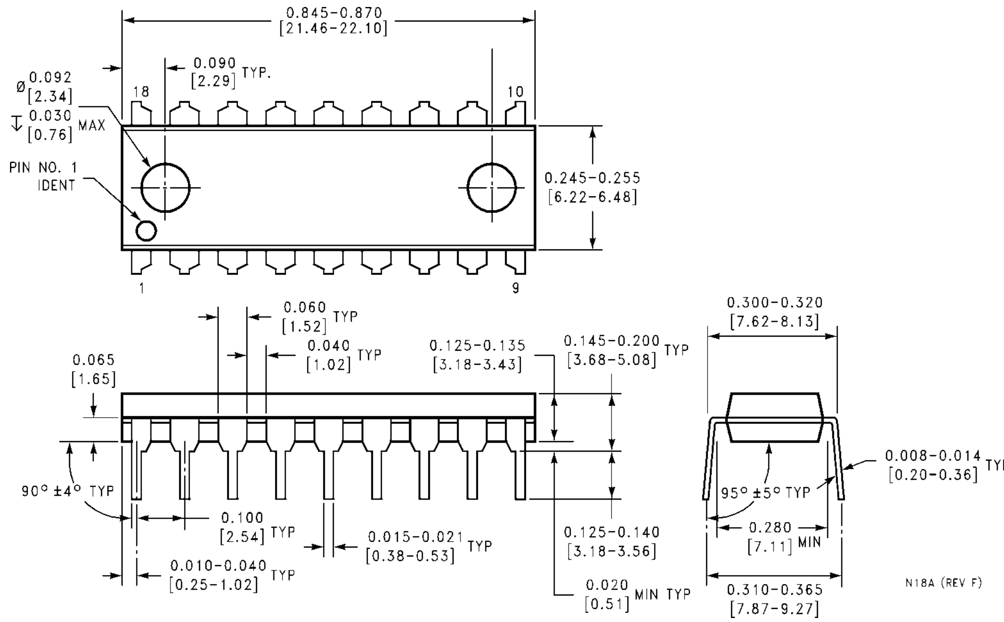


Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



18-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide
Package Number N18A

LIFE SUPPORT POLICY

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.